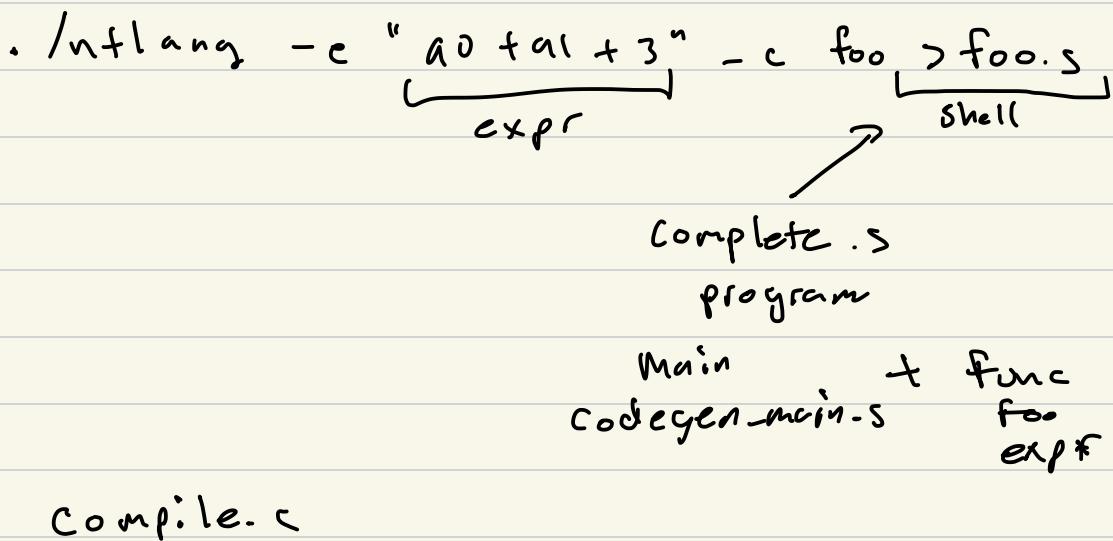


# CS 631-02 RISC-V Code Gen in Machine Code



compile-expr (tree, config)

① write out codegen-main.s

② compile\_expr-tree(tree)

↳ func:  
codegen-func.s:



ret

codegen-main.s



codegen-func.s:

add a0, a1, a2  
ret

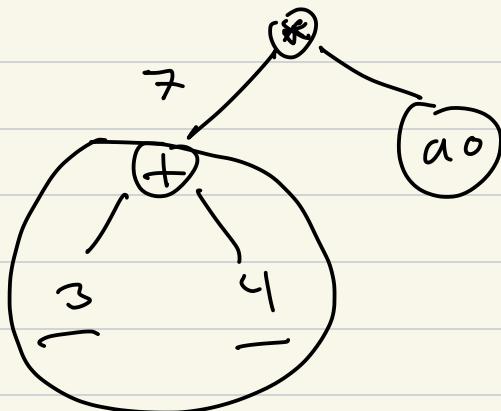
return 0

li a0, 0  
ret

---

## Constant Folding

$$(3 + 4) * a0$$



IR

## Intermediate representation

L RTL register transfer language

## Machine Code

$$2^5 = 32$$

## Binary Form of Assembly

00350533

add    ao, ao, a\  
        rd    rl    rs?

Diagram illustrating the bit fields of an R-Type instruction:

- funct7**: bits 0-6
- a1**: bit 7
- a0**: bit 8
- rs2**: bits 9-11
- rs1**: bits 12-14
- funct3**: bits 15-17
- rd**: bit 18
- opcode**: bits 19-31